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1. (currently amended) A ~~type of~~ carry look-ahead circuit ~~characterized by the fact that it is composed of~~ comprising:

at least one ~~or several~~ first logic [[gates]]gate that [[output]] outputs AND, NAND, OR or NOR of input 2-bit signals, and

at least one ~~or several~~ second logic [[gates]] gate that [[output]] outputs OR or NOR of AND of 2-bit signals among input 3-bit signals and [[the]] another [[other]] 1-bit signal, or one of AND, [[or]] NAND, [[of]] OR of 2-bit signals among input 3-bit signals and the other 1-bit signal.

2. (currently amended) A [[type of]] carry look-ahead circuit ~~characterized by the fact that it is composed of~~ comprising

at least one ~~or several~~ first logic gates that output one of AND, NAND, OR, [[or]] NOR of input 2-bit signals,

at least one ~~or several~~ second logic [[gates]] gate that output one of OR, [[or]] NOR of AND of 2-bit signals among input 3-bit signals and ~~the other~~ another 1-bit signal, or one of AND, [[or]] NAND of OR of 2-bit signals among input 3-bit signals and the other 1-bit signal,

and at least one ~~or several~~ third logic gates that output NOT of a 1-bit input.

3. (currently amended) A [[type of]] carry look-ahead circuit ~~characterized by the following facts:~~ comprising:

a ~~the carry look-ahead~~ circuit that outputs a carry generation signal corresponding to the result of an OR operation from [[the]] a first logic operation item to the Nth logic operation item for the (k - 1)th logic operation item and Nth logic operation item; [[here,]] where the (k - 1)th logic operation item is equal to an AND of the ~~various~~ positions from the Nth position to the kth position (where k is a natural number in the range of 2-N) of the input carry propagation signal and the (k - 1)th position of said input carry generation signal, with the least significant position of the input (N - 1)-bit carry propagation signal (where N is a natural

number) taken as the second position and the least significant position of the N-bit carry generation signal taken as the first position, and the Nth logic operation item is equal to the Nth position of said output carry generation signal[[;]], comprising ~~the carry look-ahead circuit has~~ the following logic gates:

at least one ~~or several~~ first logic [[gates]] gate that ~~perform~~ performs the following operation:

in the OR operation formula of N items with said first logic operation item through Nth logic operation item set side-by-side, grouping is performed with OR for every two adjacent items taken as a group item in the order from the side of said first logic operation item to the side of said Nth logic operation item; when a common item exists in the two grouped items, OR of the two items in said group item is transformed to AND of said common item and non-common item; when the number of said group items in the OR operation formula after said grouping is larger than 2, said grouping and said transformation are carried out repeatedly for said group items in the order corresponding to said number order in the OR operation formula after said grouping; the OR operation formula made of two said group items obtained in the above process is taken as the first logic formula;

among the signals corresponding to AND, NAND, OR or NOR of said input carry propagation signals of plural bits, said input carry propagation signal, and said input carry generation signal, 2-bit signals are input, and AND, NAND, OR or NOR of the input 2-bit signals is output from said at least one [[or several]] first logic gates;

and at least one ~~or several~~ second logic [[gates]] gate that ~~perform~~ performs the following operation: among the signals corresponding to the operation result for said group item, said common item, and said non-common item in said first logic formula, as well as said input carry generation signal, said input carry propagation signal, and the output signal of said first logic gates, 3-bit signals are input; among the input signals, the signal corresponding to OR or NOR of AND of 2-bit signals and the other 1-bit signal, or the signal corresponding to AND or

NAND of OR of the 2-bit signals among the input signals and the other 1-bit signals is output as the signal corresponding to the operation result (or its NOT) for said group item, said non-common item, or said output carry generation signal.

4. (currently amended) The carry look-ahead circuit described in Claim 3 ~~characterized by the following facts:~~ further comprising

the position one position lower than the second position of said input carry propagation signal is taken as the first position; and said first logic gate contains a logic gate that has the signal of the first position of said input carry propagation signal input to it, as a 1-bit signal among the input 2-bit signals;

and a logic gate that outputs the carry propagation signal [[(]]or its NOT[[)]] corresponding to the operation result of AND for the ~~various~~ positions ranging from the first position to the Nth position of said input carry propagation signal.

5. (currently amended) The carry look-ahead circuit described in Claim 3 ~~or 4 characterized by the fact that~~ wherein

it contains at least one ~~or several~~ third logic [[gates]] gate, which take the 1-bit signal among said input carry generation signal, said input carry propagation signal, the output signal of said first logic gate, and the output signal of said second logic gate as input, perform NOT for said input signal, and output the result to said first logic gate or said second logic gate, or which output [same] as said output carry propagation signal or said output carry generation signal.

6. (currently amended) ~~A type of~~ An adder ~~characterized by the fact that~~ comprising

[[the]] an adder that contains at least one ~~or several~~ carry look-ahead ~~circuits~~ circuit ~~with the following constitution: they have the following circuits:~~ comprising:

a first logic operation circuit, which outputs exclusive OR of the ~~various~~ positions of two addition object signals as the carry propagation signal, and which outputs

AND of the ~~various~~ positions of said two addition object signals as the carry generation signal,

a second logic operation circuit, which performs a carry operation for each position generated due to addition of said addition object signals corresponding to said carry propagation signal and said carry generation signal of said first logic operation circuit, and which outputs the operation result as the carry signal,

and a third logic operation circuit, which performs exclusive OR for said carry signal from the lower position with respect to each position of said addition object signal and said carry propagation signal for each position, and which outputs the operation result as the result of addition of each position;

and said second logic operation circuit contains at least one ~~or several~~ carry look-ahead ~~circuits~~ circuit composed of at least one ~~or several~~ first logic [[gates]] gate, which output one of AND[[.]], NAND, OR or NOR of input 2-bit signals, and

at least one ~~or several~~ second logic [[gates]] gate, which output OR or NOR of AND of 2-bit signals among input 3-bit signals and ~~the other~~ another 1-bit signal, or AND or NAND of OR of 2-bit signals among input 3-bit signals and the other 1-bit signal.

7. (currently amended) ~~A type of~~ An adder ~~characterized by the fact that~~ comprising

[[the]] an adder that contains at least one ~~or several~~ carry look-ahead ~~circuits~~ circuit ~~with the following constitution: they have the following circuits:~~ comprising:

a first logic operation circuit, which outputs exclusive OR of the ~~various~~ positions of two addition object signals as the carry propagation signal, and which outputs AND of the ~~various~~ positions of said two addition object signals as the carry generation signal,

a second logic operation circuit, which performs carry operation for each position generated due to addition of said addition object signals corresponding to

said carry propagation signal and said carry generation signal of said first logic operation circuit, and which outputs the operation result as the carry signal,

and a third logic operation circuit, which performs exclusive OR for said carry signal from the lower position with respect to each position of said addition object signal and said carry propagation signal for each position, and which outputs the operation result as the result of addition of each position;

and said second logic operation circuit contains at least one ~~or several~~ carry look-ahead ~~circuits~~ circuit composed of at least one ~~or several~~ first logic [[gates]]gate, which output AND[[.]], NAND, OR or NOR of input 2-bit signals,

at least one ~~or several~~ second logic [[gates]] gate, which output OR or NOR of AND of 2-bit signals among input 3-bit signals and ~~the other~~ another 1-bit signal, or AND or NAND of OR of 2-bit signals among input 3-bit signals and the other 1-bit signal, and

at least one ~~or several~~ third logic [[gates]] gate that output NOT of an input 1-bit signal.

8. (currently amended) ~~A type of~~ An adder ~~characterized by the following facts:~~ comprising:

[[the]]an adder that has the following circuits: a first logic operation circuit, which outputs exclusive OR of the ~~various~~ positions of two addition object signals as the carry propagation signal, and which outputs AND of the ~~various~~ positions of said two addition object signals as the carry generation signal,

a second logic operation circuit, which performs carry operation for each position generated due to addition of said addition object signals corresponding to said carry propagation signal and said carry generation signal of said first logic operation circuit, and which outputs the operation result as the carry signal,

and a third logic operation circuit, which performs exclusive OR for said carry signal from the lower position with respect to each position of said addition

object signal and said carry propagation signal for each position, and which outputs the operation result as the result of addition of each position;

said second logic operation circuit contains at least one ~~or several~~ carry look-ahead ~~circuits~~ circuit, which take said carry propagation signals of plural bits and said carry generation signals of plural bits output from said first logic operation circuit as input, and which output an output carry propagation 1-bit signal and an output carry generation 1-bit signal,

and a carry signal output circuit that outputs said carry signal corresponding to said carry propagation signal and said carry generation signal of said first logic operation circuit as well as said output carry propagation signal and said output carry generation signal of a said carry look-ahead circuit;

[[a]]wherein said carry look-ahead circuit ~~is characterized by the following facts:~~ comprises:

[[the]] a carry look-ahead circuit that outputs said output carry generation signal corresponding to the result of OR operation from the first logic operation item to the Nth logic operation item for the (k - 1)th logic operation item and Nth logic operation item that is equal to the Nth digit of the aforementioned input carry generating signal; [[here,]]where the (k - 1)th logic operation item is equal to AND of the ~~various~~ positions from the Nth position to the kth position (where k is a natural number in the range of 2-N) of the input carry propagation signal and the (k - 1)th position of said input carry generation signal,

with the least significant position of said N-bit carry propagation signal (where N is a natural number) input from said first logic operation circuit and the least significant position of said N-bit carry generation signal as the first positions, respectively,

and the carry look-ahead circuit outputs said output carry propagation signal corresponding to the result of operation for AND of the various positions from the first position to the Nth position of said input carry propagation signal;

wherein the carry look-ahead circuit has the following logic gates:

at least one ~~or several~~ first logic [[gates]] gate that ~~perform~~ performs the following operation:

in the OR operation formula of N items with said first logic operation item through Nth logic operation item set side-by-side, grouping is performed with OR for every two adjacent items taken as a group item in the order from the side of said first logic operation item to the side of said Nth logic operation item; when a common item exists in the two grouped items, OR of the two items in said group item is transformed to AND of said common item and non-common item; when the number of said group items in the OR operation formula after said grouping is larger than 2, said grouping and said transformation are carried out repeatedly for said group items in the order corresponding to said number order in the OR operation formula after said grouping; the OR operation formula made of two said group items obtained in the above process is taken as the first logic formula;

among the signals corresponding to AND, NAND, OR or NOR of said input carry propagation signals of plural bits, said input carry propagation signal, and said input carry generation signal, 2-bit signals are input, and AND, NAND, OR or NOR of the input 2-bit signals is output from said one or several first logic gates;

and at least one ~~or several~~ second logic [[gates]] gate that ~~perform~~ performs the following operation: among the signals corresponding to the operation result of said group item, said common item, and said non-common item in said first logic formula, as well as said input carry generation signal, said input carry propagation signal, and the output signal of said first logic gates, 3-bit signals are input; among the input signals, the signal corresponding to OR or NOR of AND of 2-bit signals and the other 1-bit signal, or the signal corresponding to AND or NAND of OR of 2-bit signals among the input signals and the other 1-bit signal is output as the signal corresponding to the operation result [[(]]or its NOT[[)]] for said group item, said non-common item, or said output carry generation signal.

9. (currently amended) The adder described in Claim 8 ~~characterized by the fact that~~ wherein the carry look-ahead

contains at least one ~~or several~~ third logic [[gates]] gate, which [[take]] takes the 1-bit signal among said input carry generation signal, said input carry propagation signal, the output signal of said first logic gate, and the output signal of said second logic gate as input, perform NOT for said input signal, and output the result to said first logic gate or said second logic gate, or which output ~~[the signal]~~ as said output carry propagation signal or said output carry generation signal.

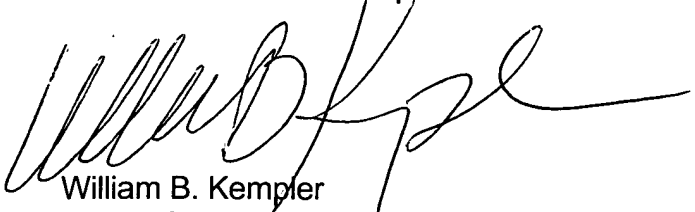
10. (currently amended) The adder described in Claim 8 ~~or 9 characterized by the following facts:~~ wherein

said plural carry look-ahead circuits are classified into plural layers;

the carry look-ahead circuits contained in the initial layer take said carry propagation signal of plural bits and said carry generation signal of plural bits output from said first logic operation circuit as inputs, and output a carry propagation 1-bit signal and carry generation 1-bit signal as outputs;

the carry look-ahead circuits in each of the layers after the initial layer take said output carry propagation signal of plural bits and said output carry generation signal of plural bits output from said plural carry look-ahead circuits in the preceding layer as inputs, and generate an output carry propagation 1-bit signal and output carry generation 1-bit signal as outputs.

Respectfully submitted,
Texas Instruments Incorporated



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